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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,145	02/07/2002	Guy E. Averett	ONS00317	1448

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ON Semiconductor
Patent Administration Dept - MD A700
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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/072,145	AVERETT ET AL.
	Examiner	Art Unit
	Ori Nadav	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,10,26,27,29,32 and 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,10,26,27,29,32 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 5-8, 10, 26, 29 and 32-33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support in the specification for the claimed limitations of a structure comprising a first dielectric material substantially fills the first trench, wherein a second trench is present in the first dielectric material and having walls, a lower surface and a second opening, as recited in claims 1 and 26, because the first dielectric material is present in only about half of the first trench.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7, 10 and 32-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of a layer of material

formed overlying the walls of the second recessed region and comprising polycrystalline as recited in claims 7, 10 and 32-33, are unclear as to whether the layer of material comprising polycrystalline is the same layer as the polycrystalline semiconductor layer, recited in independent claims 1 and 26, or a different layer.

Note that if the layer of material comprising polycrystalline is the same layer as the polycrystalline semiconductor layer, then the same element must be recited by the same name. On the other hand, if the layer of material comprising polycrystalline is a different layer from the polycrystalline semiconductor layer, then there is no support in the specification for an intermediary structure comprising a layer of material comprising polycrystalline and a polycrystalline semiconductor layer.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 5-8, 10, 26, 29 and 32-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Akatsu (6,333,274).

Regarding claims 1, 5 and 26, Akatsu teaches in figures 2I to 2O and related text an intermediary of a semiconductor device, comprising:

a semiconductor substrate having a surface formed with a first trench 49;

a first dielectric material 50 formed in the first trench, wherein the first dielectric material substantially fills the first trench;

a polysilicon polycrystalline semiconductor layer 54 formed overlying the first dielectric material 50 and having a first opening; and

a second trench etched into the first dielectric material through the first opening,

wherein the second trench has walls, a lower surface and a second opening, and wherein the first opening at least partially overlies at least partially overlying the first opening, wherein

the polycrystalline semiconductor layer and the second recessed region are configured to form a region of reduced substrate capacitance.

Regarding the claimed limitations of a second trench etched into the first dielectric material through the first opening, these are process limitations which would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this

issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding the claimed limitations of a polycrystalline semiconductor layer and the second recessed region are configured to form a region of reduced substrate capacitance, this feature is inherent in Akatsu's device, because Akatsu's structure is identical to the claimed structure.

Regarding claims 6-8, 10, 29 and 32-33, Akatsu teaches in figures 2I to 2O and related text, the first dielectric material 50 includes deposited silicon dioxide, and

a layer of material 55 formed overlying the walls of the second trench and comprising polycrystalline,

wherein the first dielectric material is recessed below a major surface of the semiconductor substrate;

wherein the second opening is wider than the first opening.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 9, as best understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Akatsu.

Regarding claim 9, Akatsu does not state that the first dielectric material is recessed below the major surface a distance of about 0.5 microns. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recess the first dielectric material below the major surface a distance of about 0.5 microns in prior art's device in order to adjust the characteristics of the device according to the requirements of the application in hand.

Response to Arguments

Applicant argues that the claimed limitations recited in claims 7, 10 and 32-33 are clear, because figure 4 depicts layer 95 as a separate layer from polycrystalline layer 75.

Although figure 4 depicts layer 95 as a separate layer from polycrystalline layer 75, the claimed limitations of a layer of material formed overlying the walls of the second recessed region and comprising polycrystalline as recited in claims 7, 10 and 32-33, are

still unclear because independent claims 1 and 26 recite a layer of material comprising polycrystalline. Dependent claims 7, 10 and 32-33 use the same names of elements, as recited in the independent claims, but without using the terms "the" or "said". Therefore, it is unclear as to whether the layer of material comprising polycrystalline is the same layer as the polycrystalline semiconductor layer, recited in independent claims 1 and 26, or a different layer.

Applicant argues that Akatsu does not teach a first dielectric material substantially fills the first trench.

Figure 4 of the present invention depicts a first dielectric material is present in only part of the first trench, since a second trench is present in the first dielectric material and having walls, a lower surface and a second opening. Akatsu also teaches a first dielectric material is present in only part of the first trench. Based on the disclosed invention, since applicant's meaning of the phrase "substantially fills" only means "part of", then Akatsu teaches a first dielectric material substantially fills the first trench.

Applicant argues that Akatsu does not teach a second trench etched into the first dielectric material through the first opening.

The claimed limitations of a second trench etched into the first dielectric material through the first opening are process limitations which would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily

produced.

Applicant argues that layer 54 of Akatsu is not configured to form a region of reduced substrate capacitance.

The claimed limitations of a polycrystalline semiconductor layer and the second recessed region are configured to form a region of reduced substrate capacitance, are inherent in Akatsu's device, because Akatsu's structure is identical to the claimed structure.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
10/18/07

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